High Performance Primary Side Regulation CV/CC Power Switch With Single Failure Protections

FEATURES

- **Built-in 800V High Voltage Power BJT**
- **Primary Side Regulation (PSR) Control with High Efficiency**
- **Single Failure Protections for power supply**
- **Multi-Mode PSR Control**
- **Fast Dynamic Response**
- **Optimized EMI Performance**
- **Audio Noise Free Operation**
- **±5% CC and CV Regulation**
- **Low Standby Power <30mW**
- **Programmable Cable Drop Compensation (CDC)**
- **Build in Protections:**
  - **Short Load Protection (SLP)**
  - **FB Over Voltage Protection (FB OVP)**
  - **Cycle-by-Cycle Current Limiting (OCP)**
  - **On-Chip Thermal Shutdown (OTP)**
  - **VDD OVP & UVP & Clamp**
- **Available with SOP-7/8 Package**

APPLICATIONS

- **Battery Chargers for Cellular Phones**
- **AC/DC Power Adapter**

GENERAL DESCRIPTION

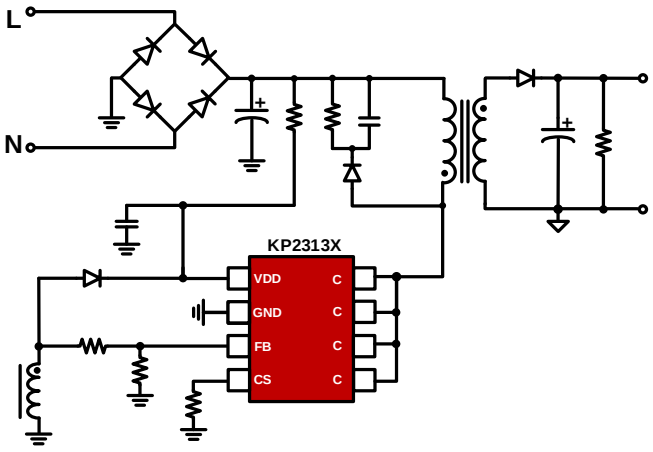
KP2313X is a high performance Primary Side Regulation (PSR) PWM power switch with high precision CV/CC control ideal for charger applications.

KP2313X can achieve audio noise free operation and fast dynamic response. The built-in Cable Drop Compensation (CDC) function can provide excellent CV performance.

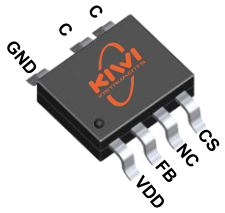
KP2313X integrates functions and protections of VDD Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), FB Over Voltage Protection (FB OVP), On-Chip Thermal Shutdown, VDD Clamping, etc.

KP2313X also integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection, R_{CS} open protection and IC GND pin open protection.

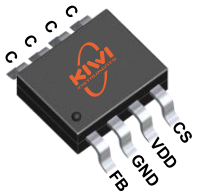
TYPICAL APPLICATION CIRCUIT



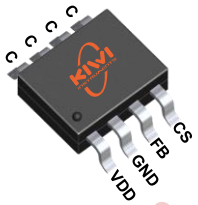
Pin Configuration



SOP-7
KP23130/1/2



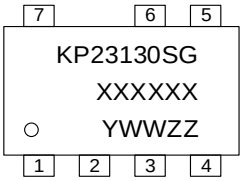
SOP-8
KP23132M/L/D, KP23130M



SOP-8
KP23132K

Marking Information

XXXXXX: Wafer Lot Code
Y: Year Code
WW: Week Code, 01-52
ZZ: Serial Number, 01-99 or A0-ZZ



SOP-7

XXXXXX: Wafer Lot Code
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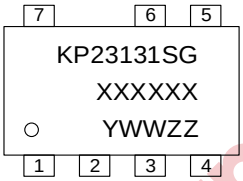

SOP-7

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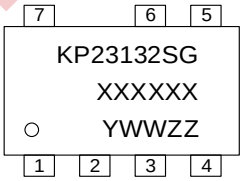

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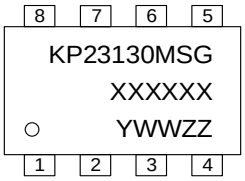

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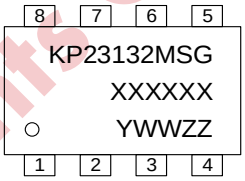

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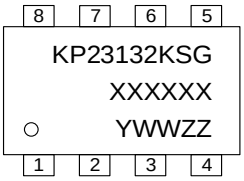

SOP-8

XXXXXX: Wafer Lot Code
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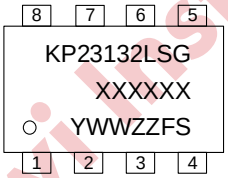
ZZ: Serial Number, 01-99 or A0-ZZ
F,S: Control Number, 1-9 or A-Z, a-z



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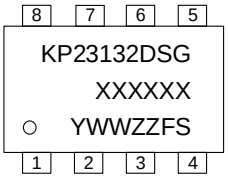


SOP-8

Typical Output Power Table(1)

Product	Package	230VAC ± 15%(2)	85-265VAC
		Charger, Adapter(3)	Charger, Adapter(3)
KP23130	SOP-7	7.5W	5W
KP23130M	SOP-8	7.5W	5W
KP23131	SOP-7	10W	7.5W

KP23132D	SOP-8	12W	10W
KP23132	SOP-7	15W	12W
KP23132M	SOP-8	15W	12W
KP23132K	SOP-8	15W	12W
KP23132L	SOP-8	15W	12W

(1) The Max output power is limited by junction temperature.

(2) 230VAC or 100/115VAC with voltage doublers.

(3) Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50˚C ambient.

Pin Description

KP23130/1/2	KP23132M/L/D KP23130M	KP23132K	Pin Name	Type(4)	Description
1	3	1	VDD	P	IC Power Supply Pin
2	1	3	FB	I	System Feedback and Demagnetization Detection Pin
3	-	-	NC	-	No Connect
4	4	4	CS	I	Current Sense Input Pin
5, 6	5, 6, 7, 8	5, 6, 7, 8	C	P	Internal Power BJT Collector Pin
7	2	2	GND	G	IC Ground Pin

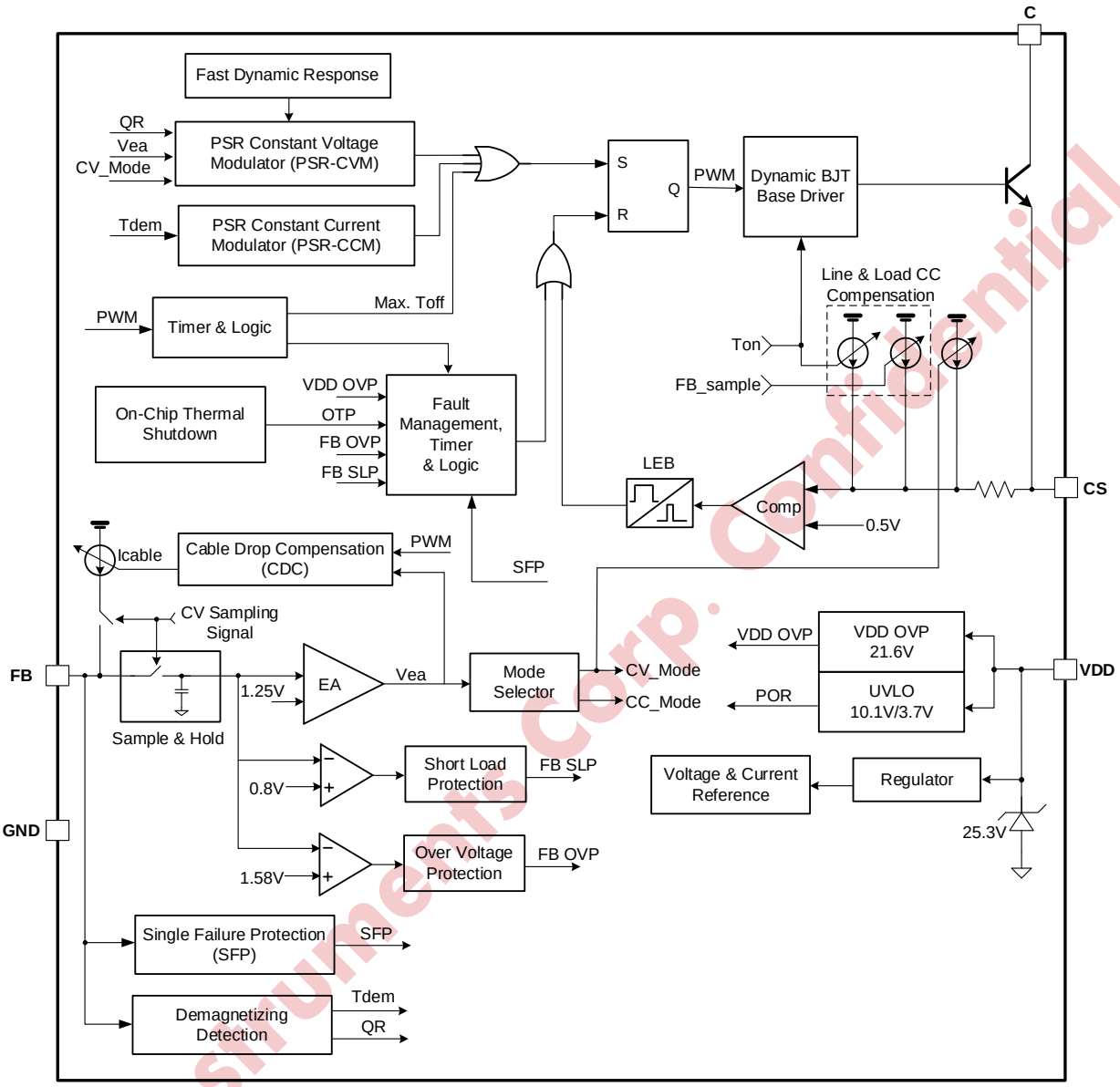
(4) I-Input； P-Power；G-Ground.

Ordering Information

Part Number(5)	Description
KP23130SGA	SOP-7, Halogen free, in T&R, 4000 Pcs/Reel
KP23131SGA	SOP-7, Halogen free, in T&R, 4000 Pcs/Reel
KP23132SGA	SOP-7, Halogen free, in T&R, 4000 Pcs/Reel
KP23132DSGA	SOP-8, Halogen free, in T&R, 4000 Pcs/Reel
KP23130MSGA	SOP-8, Halogen free, in T&R, 4000 Pcs/Reel
KP23132MSGA	SOP-8, Halogen free, in T&R, 4000 Pcs/Reel
KP23132KSGA	SOP-8, Halogen free, in T&R, 4000 Pcs/Reel
KP23132LSGA	SOP-8, Halogen free, in T&R, 4000 Pcs/Reel

(5) Suffix "A" – Tape & Reel, “M” and “K” presents two types of Pin Configuration.

Block Diagram



Absolute Maximum Ratings(6)

Parameter		Value	Unit
C Pin Voltage Range		-0.3 to 800	V
VDD DC Supply Voltage		-0.3 to 33	V
VDD DC Clamp Current		10	mA
CS Voltage Range		-0.3 to 6	V
FB Voltage Range		-0.7 to 6	V
Package Thermal Resistance---Junction to Ambient (SOP-7/8)		165	˚C/W
Maximum Junction Temperature		165	˚C
Storage Temperature Range		-40 to 165	˚C
Lead Temperature (Soldering, 10sec.)		260	˚C
ESD Capability, HBM (Human Body Model) (7)		5	kV
ESD Capability, CDM (Charged Device Model)(8)		2	kV
Maximum DC Collector Current	KP23130(M)	0.8	A
	KP23131	2	A
	KP23132D	2.5	A
	KP23132(M/K/L)	4	A
Maximum pulse Collector Current	KP23130(M)	1.6	A
	KP23131	4	A
	KP23132D	5	A
	KP23132(M/K/L)	8	A

(6) Stresses listed as the above “Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

(7) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(8) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, VDD	5 to 19	V
Chip Operating Junction Temperature	-40 to 125	˚C
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

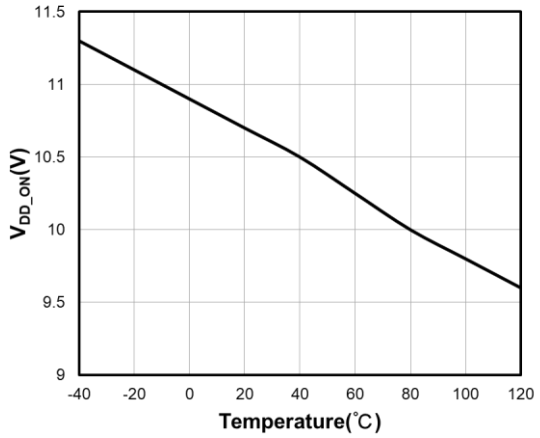
Electrical Characteristics (T_A= 25℃, VDD=16V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage Section (VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin	VDD< V_{DD_ON}	0.1	1.5	3	μA
I_{VDD_Q}	Quiescent Current		130	195	230	μA
V_{DD_ON}	VDD Under Voltage Lockout Exit		9	10.1	11	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter(9)			3.7		V
V_{DD_OVP}	VDD OVP Threshold		20	21.6	23.5	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	I(V_{DD}) >5 mA	23.5	25.3	27	V
Control Function Section (FB Pin)						
V_{FBREF}	Internal Error Amplifier (EA) Reference Input		1.24	1.25	1.26	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold(9)			0.8		V
V_{FB_OVP}	FB Over Voltage Protection Threshold		1.5	1.58	1.7	V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time(9)			38		ms
T_{FB_OVP}	FB Over Voltage Protection Debounce Time			3		Tsw
V_{FB_DEM}	Demagnetization Comparator Threshold (before start up)	Upper Threshold (9)		30		mV
		Lower Threshold (9)		-20		mV
	Demagnetization Comparator Threshold (after start up)	Upper Threshold (9)		40		mV
		Lower Threshold (9)		-100		mV
T_{blank}	Leading Edge Blanking Time	CC Mode		4		μs
		CV Mode		2		μs
T_{on_max}	Maximum ON time(9)			25		μs

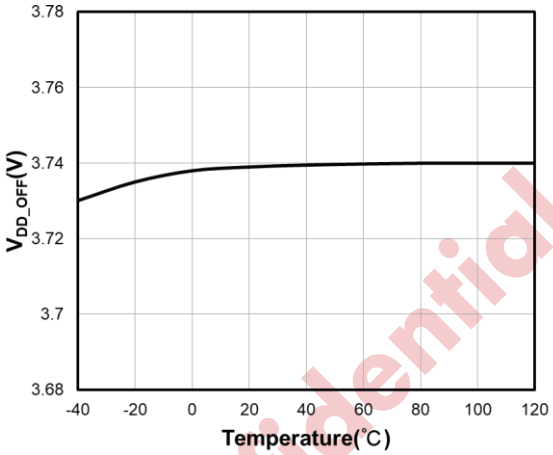
T_{off_max}	Maximum OFF time(9)			6		ms
I_{Cable_max}	Maximum Cable Drop Compensation(CDC) Current		14.6	15.85	17.4	μA
K_{CC}	Ratio between Switching Period and Demagnetization Time in CC Mode(9)	KP23132L		7/4		
		Others		2		
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time(9)			455		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
$V_{cs(min)}$	Current limiting threshold		205	233	255	mV
T_{D_OC}	Over Current Detection and Control Delay			100		ns
On-Chip Thermal Shutdown						
T_{SD}	Thermal Shutdown(9)			155		˚C
T_{RC}	Thermal Recovery(9)			125		˚C
Power BJT Section (C Pin)						
V_{CBO}	Collector-Base Breakdown Voltage(6)		800			V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	KP23130(M) (I_C=0.1A, I_b=20mA)			0.5	V
		KP23131 (I_C=0.5A, I_b=0.1A)			0.25	V
		KP23132D (I_C=0.5A, I_b=0.1A)			0.4	V
		KP23132(M/K/L) (I_C=1A, I_b=0.2A)			0.4	V
h_{FE}	DC Current Gain		20		30	

(9) Guaranteed by the Design.

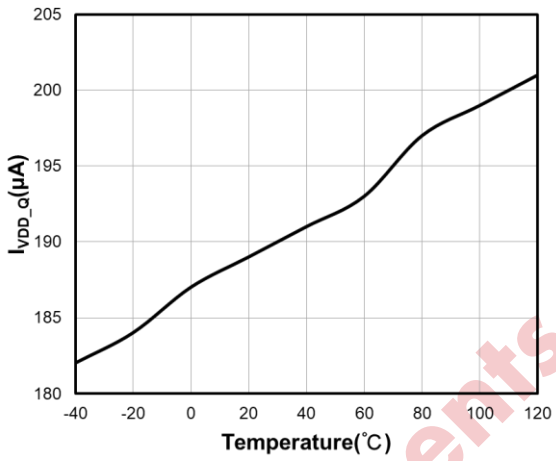
Typical Characteristic



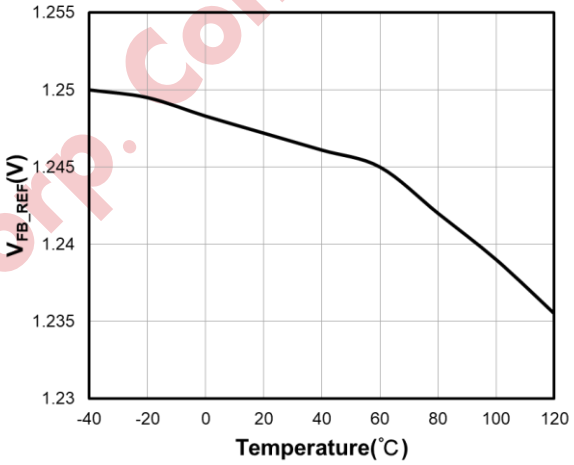
V_{DD_ON} vs Temperature



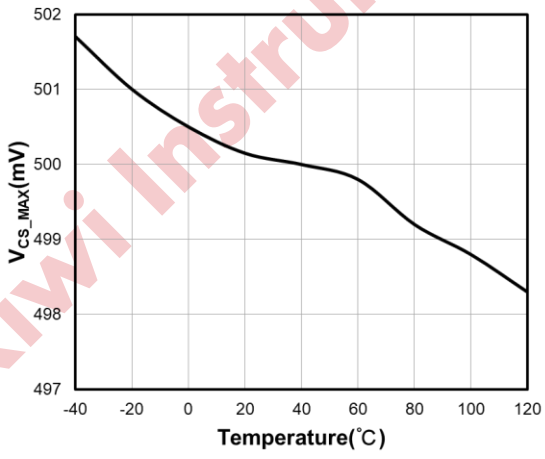
V_{DD_OFF} vs Temperature



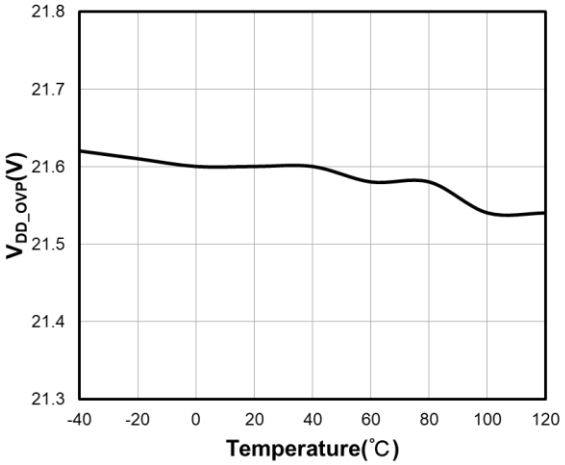
I_{VDD_Q} vs Temperature



V_{FB_REF} vs Temperature



V_{CS_MAX} vs Temperature



V_{DD_OVP} vs Temperature

Operation Description

KP2313X is a high performance, multi-mode, Primary Side Regulation (PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

System Start-Up Operation

Before the IC starts to work, it consumes only startup current I_{VDD_st}, (1.5μA typically) which allows a large value startup resistor to be used to minimize the standby power loss. When VDD reaches turn-on voltage V_{DD_on}, (10.1V typically), KP2313X begins switching. The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes control.

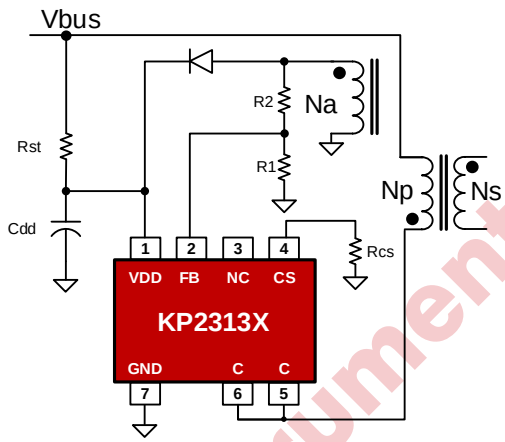


Fig 1

Once KP2313X enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced, which helps to reduce the standby power loss.

PSR CV Modulation (PSR-CVM)

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Fig.2 illustrates the timing waveform of CV sampling signal, demagnetization signal (DEM). When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the PSR CV Modulator (PSR-CVM) for CV regulation. The internal reference voltage for EA is trimmed to V_{FB_REF} (1.25V typically).

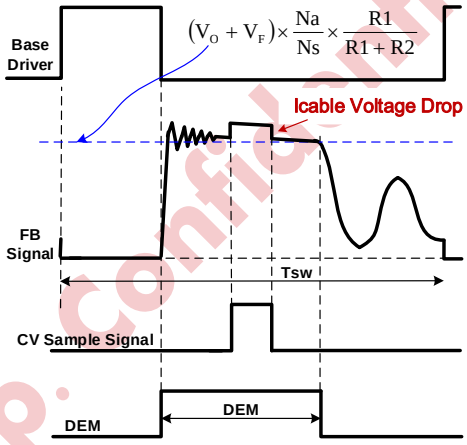


Fig 2

During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, as shown in Fig.2. Fig.2 also illustrates the equation for “demagnetization plateau”,

$$V_{FB} = (V_O + V_F) \times \frac{Na}{Ns} \times \frac{R1}{R1+R2}$$

Where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na is secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as shown in “Block Diagram”) based on EA output will switch to CC Mode automatically.

● PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp (max), as shown in Fig.3.

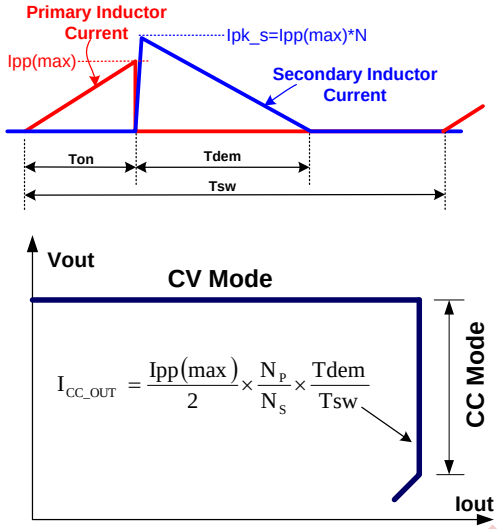


Fig 3

Referring to Fig.3 above, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown in Fig.3. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the IC operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

In KP2313X, the ratio between Tdem and Tsw in CC mode is K_{cc}. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(\text{mA}) \cong \frac{1}{2} \times \frac{1}{K_{CC}} \times N \times \frac{500\text{mV}}{\text{Rcs}(\Omega)}$$

In the equation above,

N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power BJT emitter to GND.

● Multi-Mode Control in CV Mode

To meet the tight requirement of averaged system efficiency and no-load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in KP2313X which is shown in the Fig 4.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 30mW.

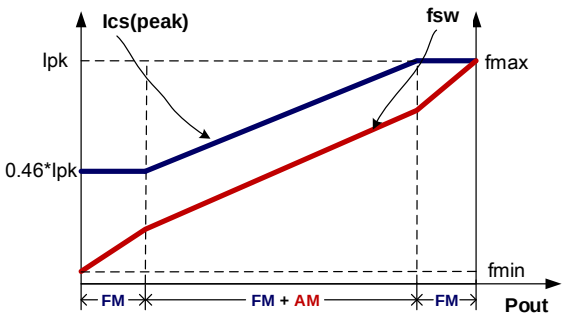


Fig 4

● Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire

which can cause several percentages of voltage drop on the actual battery voltage. In KP2313X, an offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig.5) flowing into the resistor divider. The current is proportional to the switching period; thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. The percentage of maximum compensation is given by

$$\frac{\Delta V(\text{cable})}{\text{Vout}} \approx \frac{\text{Icable\_max} \times (\text{R1}//\text{R2})}{V_{\text{FB\_REF}}} \times 100\%$$

For example, R1=5KΩ, R2=40KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(\text{cable})}{\text{Vout}} \approx \frac{15.85u \times (40\text{k}//5\text{k})}{1.25} \times 100\% = 5.64\%$$

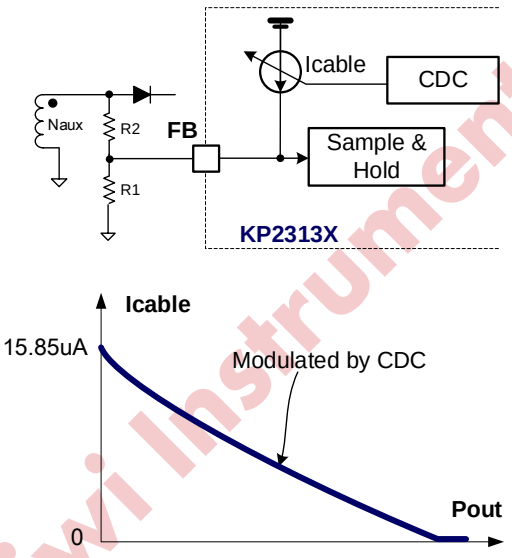


Fig 5

Fast Dynamic Response

In KP2313X, the dynamic response performance is optimized to meet USB charge requirements.

Single Failure Protections for Power Supply

KP2313X integrates single failure protections, including FB pull-up resistor open protection, FB pull-down resistor open protection, FB pull-down resistor short protection, output rectifier diode or SR open protection, output rectifier diode or SR short protection, transformer windings short protection, R_{CS} open protection and IC GND pin open protection. This function can ensure there is no damage to IC and no over voltage of output.

On Chip Thermal Shutdown (OTP)

When the IC temperature is over T_{SD} (155 ˚C typically), the IC shuts down. Only when the IC temperature drops to T_{RC} (125˚C typically), IC will restart.

Audio Noise Free Operation

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation is used in CV mode. An internal current source flowing to CS pin makes CS peak voltage modulation realized. In KP2313X, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Dynamic BJT Base Drive

KP2313X integrates a dynamic base drive control to optimize efficiency. The BJT base drive current is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current.

Short Load Protection (FB SLP)

In KP2313X, the output is sampled on FB pin and then compared with V_{FB_SLP} (0.8V typically).

In KP2313X, when sensed FB voltage is below

V_{FB_SLP} and hold T_{FB_short} (38ms typically), the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

- **FB Over Voltage Protection (FB OVP)**

In KP2313X, the output is sampled on FB pin and then compared with V_{FB_OVP} (1.58V typically).

When sensed FB voltage is above V_{FB_OVP} for more than 3 cycles, the IC will enter into Over Voltage Protection (OVP) mode, in which the IC will enter into auto recovery protection mode.

- **VDD Over Voltage Protection (OVP) and Zener Clamp**

When VDD voltage is higher than V_{DD_OVP} (21.6V typically), the IC will stop switching. This will cause VDD fall down to be lower than V_{DD_OFF} (3.7V typically) and then the system will restart up again. An internal Zener clamp is integrated to prevent the IC from damage, and the clamp voltage is V_{DD_Clamp} (25.3V typically).

Application Information

- **PCB Layout Guidelines**

PCB design has a significant impact on the performance of power supply. It is recommended to refer to Figure 6 and Figure 7 when designing primary-side circuit.

1. The main power Loop (Loop1) should be as small as possible and the trace should be wide for better efficiency performance.

2. The snubber circuit Loop (Loop2) should be as small as possible.

3. Place VDD capacitor C3 close to the IC to ensure the VDD loop (Loop3) is small.

4. The ground node of auxiliary winging should be connected directly to the negative node of the bus capacitor (Line1 as shown in Fig.6)

5. VDD capacitor C3 and FB pull-down resistor R5 should be connected directly to the IC GND pin firstly, and then connects them to the negative node of the bus capacitor with a single point (Line2 as shown in Fig.6)

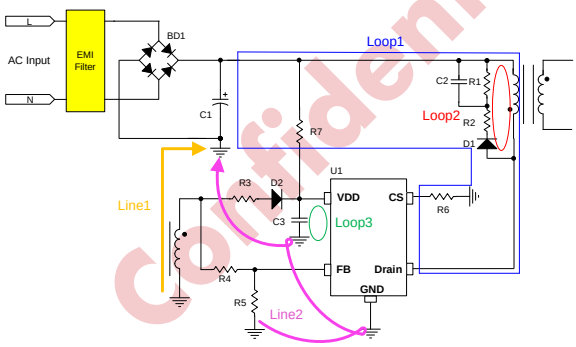


Fig 6

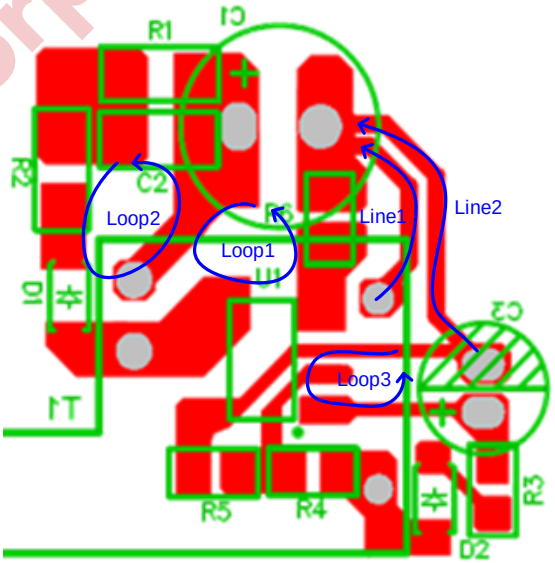
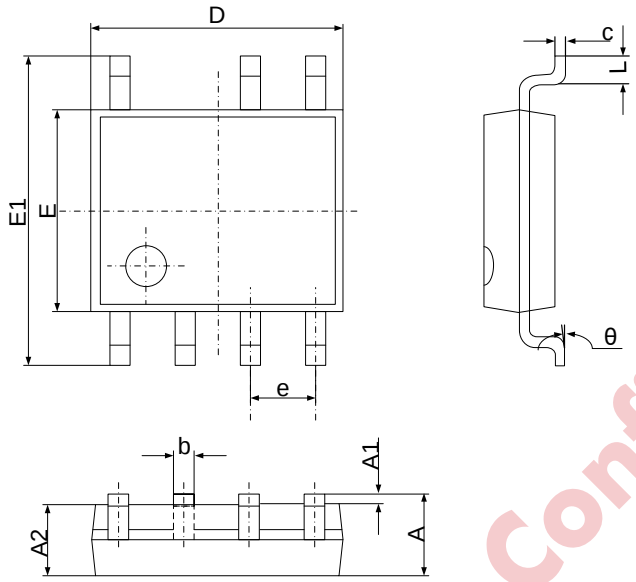


Fig 7

Package Dimension

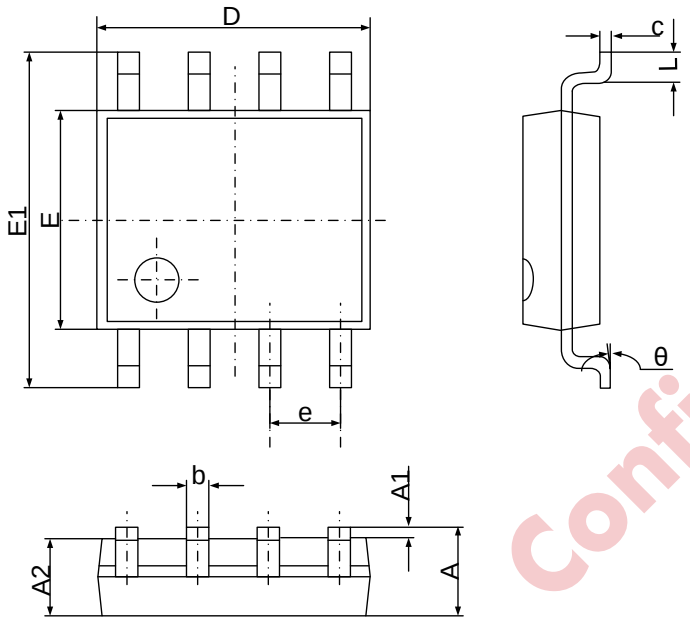
SOP-7



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Dimension

SOP-8



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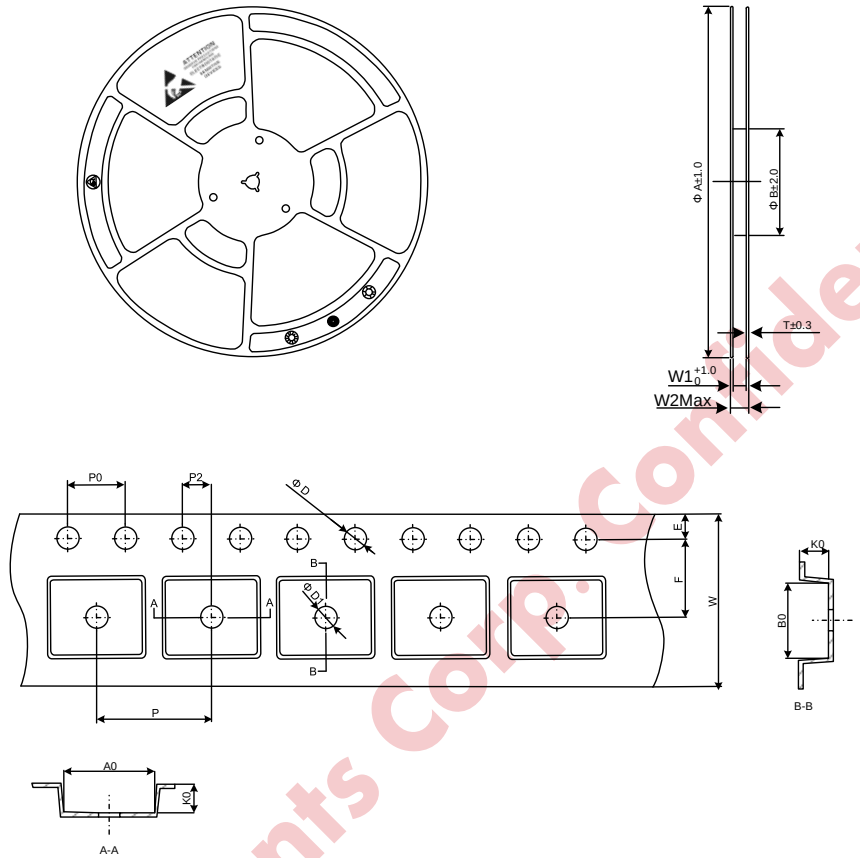
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Tape and Reel Information

SOP-7 / SOP-8



Reel Dimensions (mm)				
A	**B (Inner Diameter)**	**W1**	**W2Max**	**T**
330	100	12.4	18.4	1.5

Tape Dimensions			
Symbol	**Dimensions (mm)**	**Symbol**	**Dimensions (mm)**
E	1.75±0.10	W	12.00±0.10
F	5.50±0.10	P	8.00±0.10
P2	2.00±0.10	A0	6.60±0.10
D	$1.50^{+0.1}_{-0}$	B0	5.30±0.10
D1	1.55±0.05	K0	1.90±0.10
P0	4.00±0.10		

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